UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,728	12/16/2003	Murthi Nanja	30320/17593	3550

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EXAMINER
CHANG, ERIC

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/736,728	NANJA, MURTHI
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
   Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-21 are pending.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-4, 6-8, 11-17 and 19-20 are rejected under 35 U.S.C. 102(e) as being clearly

anticipated by U.S. Patent 6,711,447 to Saeed.

4.   As to claim 1, Saeed discloses an article comprising a machine-accessible medium

having stored thereon instructions that, when executed by a machine, cause the machine to:

obtain from a performance monitor runtime performance data indicative of a thread-level

utilization [col. 2, lines 7-13]; and based on the performance data, adjust an operating voltage or

an operating frequency of the machine [col. 2, lines 46-51].

5.   As to claim 2, Saeed discloses the performance monitor [210] is a Performance

Monitoring Unit (PMU) [col. 3, lines 11-22].

6.   As to claim 3, Saeed discloses the PMU is part of a central processing unit (CPU) [200]

within the machine [col. 3, lines 8-11].

7.   As to claim 4, Saeed discloses the PMU includes a plurality of counters for measuring

different performance data [col. 2, lines 19-20].

8.   As to claim 6, Saeed discloses that in response to the performance data, determining if

the operating voltage and operating frequency should be adjusted upward or scaled down [col. 4,

lines 5-15].

9.   As to claim 7, Saeed discloses comparing the performance data to a voltage and

frequency scheduler lookup table that stores at least one voltage value and at least one frequency

value [col. 4, lines 10-15].

10.   As to claim 8, Saeed discloses obtaining a plurality of runtime performance data [col. 2,

lines 19-26]; and in response to the plurality of runtime performance data, adjusting the

operating voltage and the operating frequency [col. 2, lines 46-51].

11.   As to claim 11, Saeed discloses operating the performance monitor in an operating

system environment in communication with a platform hardware environment [col. 3, lines 26-

31], and in communication with an end user code, in a user mode [col. 3, lines 60-64].

12.   As to claim 12, Saeed discloses adjusting the operating voltage and the operating

frequency [col. 2, lines 60-62].

13.   As to claim 13, Saeed discloses a method comprising: obtaining, from a performance

monitor, runtime performance data indicative of a thread-level utilization for a central processing

unit (CPU) having an operating voltage and an operating frequency [col. 2, lines 7-13]; in

response to the runtime performance data, determining if either the operating voltage or the

operating frequency is at a desired value [col. 4, lines 10-15]; and in response to the

determination, adjusting the operating voltage or the operating frequency [col. 2, lines 46-51].

14.   As to claim 14, Saeed discloses adjusting both the operating voltage and the operating

frequency [col. 2, lines 60-62].

15.   As to claim 15, Saeed discloses adjusting the operating voltage and the operating

frequency upward [col. 4, lines 5-15].

16.   As to claim 16, Saeed discloses adjusting the operating voltage and the operating

frequency downward [col. 4, lines 5-15].

17.   As to claim 17, Saeed discloses the performance monitor [210] is a Performance

Monitoring Unit (PMU) [col. 3, lines 11-22].

18.   As to claim 19, Saeed discloses the performance data to a voltage and frequency

scheduler lookup table that includes at least one voltage value and at least one frequency value

[col. 4, lines 10-15].

19.   As to claim 20, Saeed discloses benchmarking the CPU [col. 2, lines 7-13]; determining

the at least one voltage value and the at least one frequency value in response to the

benchmarking [col. 2, lines 47-51]; and creating a lookup table of the at least one voltage value

and the at least one frequency value [col. 2, lines 6-7 and col. 4, lines 10-15].

Claim Rejections - 35 USC § 103

20.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

21.   Claims 5, 9-10, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent 6,711,447 to Saeed in view of U.S. Patent 6,233,690 to Choi, et al.

22.   As to claim 5, Saeed teaches the limitations of the claim, including monitoring

performance data indicative of thread-level utilization, but does not teach that additional runtime

performance data includes cache misses and other data dependency stalls.

Choi teaches that a computer can have its voltage or frequency adjusted due to the monitoring of performance data [col. 1, lines 11-45]. Thus, Choi teaches a performance-based voltage and frequency adjustment similar to that of Saeed. Choi further teaches that the runtime performance data is selected from the group consisting of instruction cache misses, data cache misses, instructions executed, stalls due to data dependency, and data cache write-backs [col. 2, lines 62-67, and col. 3, lines 1-10]. Other stall conditions well known in the art comprise branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses and data translation look-up buffer TLB misses.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ additional runtime performance data as taught by Choi. One of ordinary skill in the art would have been motivated to do so that power can be saved through the monitoring of processor performance data.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of adjusting processor voltage or frequency due to the monitoring of performance data. Moreover, the additional runtime performance data means taught by Choi would improve the efficiency of Saeed because it allowed for power-saving during long latency machine stalls [col. 2, lines 62-64].

23.   As to claim 9, Choi discloses the performance data is an instructions-per-cycle metric [col. 1, lines 40-45].

24.   As to claim 10, Choi discloses the performance data is a memory references-per-cycle

metric [col. 3, lines 11-21].

25.   As to claim 18, Choi discloses the runtime performance data is selected from the group

consisting of instruction cache misses, data cache misses, instructions executed, branches

executed, branch mis-predicts, instruction translation look-up buffer misses, data translation

look-up buffer misses, stalls due to data dependency, and data cache write-backs [col. 2, lines

62-67, and col. 3, lines 1-10].

26.   As to claim 21, Choi discloses adjusting the operating voltage or the operating frequency

in response to an instructions-per-cycle metric or a memory-references-per-cycle metric [col. 1,

lines 40-45, and col. 3, lines 11-21].

Response to Arguments

27.   Applicant's arguments filed August 21, 2006 have been fully considered but they are not

persuasive.

28.   In the remarks, applicants argued in substance that Saeed does not teach or suggest that

thread-level utilization. But Saeed teaches monitoring runtime performance data indicative of a

thread-level utilization [col. 2, lines 7-13]; and based on the performance data, adjust an

operating voltage or an operating frequency of the machine [col. 2, lines 46-51]. Specifically,

Saeed teaches monitoring whether individual threads are operating as part of single or multi-

threaded applications [col. 2, lines 1-26], thereby determining overall machine performance from usage.

30. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "thread-level utilization [comprising] performance characteristics or usage patterns of individual threads running on the CPU") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

30. In the remarks, applicants argued in substance that Saeed does not teach or suggest that additional runtime performance data includes cache misses and other data dependency stalls. But Saeed teaches adjusting an operating voltage or an operating frequency of the machine [col. 2, lines 46-51] based on a detected workload [col. 2, lines 7-13]. In addition, Choi teaches that a computer can have its voltage or frequency adjusted due to the monitoring of performance data [col. 1, lines 11-45], such as instruction cache misses, data cache misses, instructions executed, stalls due to data dependency, and data cache write-backs [col. 2, lines 62-67, and col. 3, lines 1-10]. Other stall conditions well known in the art comprise branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses and data translation look-up buffer TLB misses. It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of adjusting processor voltage or frequency due to the monitoring of performance data; thus, Saeed and Choi

teach adjusting operating voltage and frequency based on such performance metrics during

thread execution.

31.   In the remarks, applicants argued in substance that Saeed does not teach or suggest a

power control circuit to monitor runtime performance. But Choi teaches circuitry for monitoring

thread performance [FIG. 2] in order to adjust power consumption [col. 1, lines 11-45].

32.   In the remarks, applicants argued in substance that Choi does not teach or suggest

adjusting a computer voltage or frequency due to the monitoring of performance data. But Choi

teaches that reducing power due to detected performance [col. 1, lines 11-45]. By gating the

clock signal, Choi teaches a reduction in the voltage consumed by the computer; likewise, the

frequency is inherently changed by the gating of the clock signal. Furthermore, Saeed teaches

other methods of adjusting the operating voltage and the operating frequency [col. 2, lines 60-

62], thereby allowing the CPU to continue to be available to process instructions or perform

calculations.

33.   In the remarks, applicants argued in substance that Choi does not teach or suggest

modulating the processor voltage or frequency, depending on how many instructions are being

performed per cycle. But Choi teaches reducing processor voltage when there are no instructions

being performed during a cycle [col. 1, lines 40-45]. Likewise, Choi discloses reducing

processor voltage based on memory references-per-cycle [col. 3, lines 11-21]. Although the,

Choi clearly teaches circuitry for detecting instructions and memory references in the processor

pipeline even while the execution logic itself may be in a low-power mode [col. 1, lines 40-45].
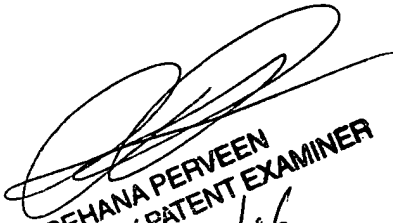

Conclusion

34.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The

examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ec

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10/30/06